CLAIMS

What is claimed is:

1. An integrated circuit fabrication method, comprising the steps of:
   (a.) providing a partially fabricated integrated circuit structure;
   (b.) applying and curing spin-on glass, to form a first dielectric;
   (c.) depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer;
   (d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers;
   (e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure;
   (f.) deposition of an interlevel dielectric;
   (g.) etching holes in said interlevel dielectric in predetermined locations; and
   (h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

2. The method of Claim 1, wherein said deposition step (c.) is plasma-enhanced.

3. The method of Claim 1, wherein said deposition step (c.) uses TEOS as a source gas.

4. The method of Claim 1, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

5. The method of Claim 1, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

6. The method of Claim 1, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

7. The method of Claim 1, wherein said interlevel dielectric is a doped silicate glass.

8. An integrated circuit fabrication method, comprising the steps of:
   (a.) providing a partially fabricated integrated circuit structure;
   (b.) applying and curing spin-on glass, to form a first dielectric;
   (c.) depositing silicon dioxide under vacuum conditions, to form a second dielectric layer over said first layer;
   (d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers;
   (e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure;
   (f.) deposition of an interlevel dielectric;
   (g.) etching holes in said interlevel dielectric in predetermined locations; and
   (h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

9. The method of Claim 8, wherein said deposition step (c.) is plasma-enhanced.

10. The method of Claim 8, wherein said deposition step (c.) uses TEOS as a source gas.

11. The method of Claim 8, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

12. The method of Claim 8, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

13. The method of Claim 8, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

14. The method of Claim 8, wherein said interlevel dielectric is a doped silicate glass.

15. An integrated circuit fabrication method, comprising the steps of:

(a.) providing a partially fabricated integrated circuit structure;

(b.) applying and curing spin-on glass, to form a first dielectric layer;

(c.) depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer, said second dielectric layer having a thickness equal to or less than said first layer;

(d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers, said third dielectric layer having a thickness equal to or greater than said second layer;

(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure;

(f.) deposition of an interlevel dielectric;

(g.) etching holes in said interlevel dielectric in predetermined locations; and

(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

16. The method of Claim 15, wherein said deposition step (c.) is plasma-enhanced.

17. The method of Claim 15, wherein said deposition step (c.) uses TEOS as a source gas.

18. The method of Claim 15, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

19. The method of Claim 15, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

20. The method of Claim 15, wherein said interlevel dielectric is a doped silicate glass.

21. The method of Claim 15, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000Å inclusive.

22. An integrated circuit manufactured by the method of Claim 1.

23. An integrated circuit manufactured by the method of Claim 8.

24. An integrated circuit manufactured by the method of Claim 15.

25. An integrated circuit, comprising:

(a.) an **active device structure,** including therein a substrate, active device structures, isolation structures, and one or more patterned thin film conductor layers including an uppermost conductor layer; and

(b.) a **planarization structure,** overlying recessed portions of said active device structure, comprising a layer of sol-gel-deposited dielectric overlain by a layer of vacuum-deposited dielectric overlain by a further layer of sol-gel-deposited dielectric;

(c.) an **interlevel dielectric** overlying said planarization structure and said active device structure, and having **via holes** therein which extend to selected locations of said uppermost conductor layer; and

(d.) an **additional thin-film patterned conductor** layer which overlies said interlevel dielectric and extends through said via holes to said ~~selectred~~ selected locations of said uppermost conductor layer.